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AMENDMENT TRANSMITTAL LETTER			Docket No. SON-1199/DIV
Application No. 09/866,662-Conf. #6271	Filing Date Concurrently Herewith	Examiner M. Prenty	Art Unit 2822

Applicant(s): Hideaki Kuroda

Invention: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

TO THE COMMISSIONER FOR PATENTS

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated and is transmitted as shown below.

CLAIMS AS AMENDED					
	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	4	- 20 =		x	0.00
Independent Claims	2	- 3 =		x	0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					
Other fee (please specify):					
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:					0.00

- ☒ Large Entity ☐ Small Entity
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- ☐ Please charge Deposit Account No. _____ in the amount of \$ _____.
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- ☒ Credit any overpayment.
- ☒ Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.

Ronald P. Kangen
Attorney Reg. No.: 24,104
RADER, FISHMAN & GRAUER PLLC
1233 20th Street, N.W.
Suite 501
Washington, DC 20036
(202) 955-3750

Dated: June 10, 2003

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Docket No.: SON-1199/ETV
(PATENT)

#9/Reg for
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a700d
6/18/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Hideaki Kuroda

Application No.: 09/866,662

Group Art Unit: 2822

Filed: May 30, 2001

Examiner: M. Prenty

For: SEMICONDUCTOR DEVICE AND METHOD
OF MANUFACTURING THE SAME

REQUEST FOR RECONSIDERATION

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action dated April 15, 2003 (Paper No. 8), Applicant respectfully requests that the above-identified patent application be reconsidered in view of the remarks that follow, that each of the presently pending claims be allowed, and that the application be passed to issue.

REMARKS

Rejections Under 35 U.S.C. §102

In the aforementioned Office Action, claims 3-6 were rejected under 35 U.S.C. §102 as anticipated by *Applicant's Prior Art Figs. 4-17 (APAF)*.

Claim 3 recites a semiconductor device, comprising a conductive layer pattern formed on a substrate; an inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate; a first connection hole formed in an upper layer of said inter-layer insulating film above said conductive layer pattern; a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said inter-layer insulation

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film; a plug having conductivity formed in a state filling internal portions of said first connection hole and said second connection hole; an upper insulating film formed on said inter-layer insulating film; a third connection hole which reaches said plug and is formed on said inter-layer insulating film; and a conductive portion which is connected to said plug and formed in said third connection hole.

Claim 4 recites a semiconductor device, comprising a conductive layer pattern formed on a substrate; an inter-layer insulating film which covers said conductive layer pattern and is formed on said substrate; a first connection hole formed in an upper layer of said inter-layer insulating film above said conductive layer pattern; a second connection hole which reaches said conductive layer pattern from the bottom portion of said first connection hole and then has a smaller diameter than that of said first connection hole and formed on said inter-layer insulation film; a plug having conductivity formed in a state filling internal portions of said first connection hole and said second connection hole, wherein the upper surface of said plug is formed to almost the same height as the surface height of said inter-layer insulating film; an upper insulating film formed on said inter-layer insulating film; a third connection hole which reaches said plug and is formed on said inter-layer insulating film; and a conductive contact portion which is connected to said plug and formed in said third connection hole.

APAF illustrates a conventional method of manufacturing a capacitor-over-bit-line (COB) type dynamic random access memory (DRAM). The method includes forming an oxide film 120 on a substrate having an N-well and P-well for element isolation. A gate electrode 131 is formed on the oxide film 120. A side wall 132 is formed and used as a mask to form a source and drain region 112. Side wall 132 is removed, and an etching stopper silicon nitride film 153 is formed on the entire top surface. A polysilicon film 133 is deposited to form apertures for the bit contacts and node contacts through resist patterning. The polysilicon film 133 is etched back to form a side wall 134. Using the polysilicon film 133 and the side wall 134 as a mask, a shrunken bit line contact hole BCH and node contact hole NCH are formed by etching. Polysilicon film 135 is used to fill the BCH and NCH contact holes so that a polyplug 136 for middle takeout is formed.

As noted above, claim 3 recites, among other things, a plug having conductivity formed in a state filling internal portions of said first connection hole and said second connection hole. *APAF* fails to disclose, teach, or suggest at least the aforementioned claim element. Instead, in

Fig. 17, *APAF* depicts that plug 136 is rectangular. Moreover, the cross-hatched shading of plug 136 is different from the areas located immediately above and below plug 136. This shading characteristic indicates that these areas are not consistent with or are a portion of plug 136. Thus, the plug 136 of *APAF*, at best, illustrates a plug filling either a first or second connection hole but not both. Further, as disclosed in the specification at page 6, line 6, the plug 136 is formed when a polysilicon film 135 is deposited into contact holes BCH and NCH. This portion of the specification provides further evidence that the plug 136 is formed in one connection hole.

To properly anticipate a claim, the document must disclose, explicitly or implicitly, each and every feature recited in the claim. See Verdegall Bros. v. Union Oil Co. of Calif., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). *APAF* fails to disclose, teach, or suggest at least a plug having conductivity formed in a state filling internal portions of said first connection hole and said second connection hole. For at least this reason, Applicant submits that *APAF* fails to anticipate claim 3. Thus, Applicant respectfully requests that the rejection of claim 3 be withdrawn, and this claim be allowed.

Based on the foregoing discussion, Applicant further submits that the Office Action has also not established that *APAF* anticipates independent claim 4. Likewise, Applicant respectfully requests that the rejection of claim 4 under 35 U.S.C. §102 be withdrawn, and claim 4 be allowed.

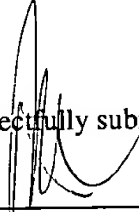
Claim 5 depends from claim 3 and claim 6 depends from claim 4. By virtue of this dependency, Applicant submits that claims 5 and 6 are allowable for at least the same reasons given above. Moreover, claims 5 and 6 are further distinguished over *APAF* by the additional features recited therein, respectively, and particularly within each claim combination.

Conclusion

Based on at least the foregoing amendments and remarks, Applicant submits that claims 3-6 are allowable, and this application is in condition for allowance. Accordingly, Applicant requests favorable reexamination and reconsideration of the application. In the event the Examiner has any comments or suggestions for placing the application in even better form, Applicant requests that the Examiner contact the undersigned attorney at the number listed below.

Dated: June 10, 2003

Respectfully submitted,

By 

Ronald P. Kananen
Registration No.: 24,104
Attorney for Applicant

RADER, FISHMAN & GRAUER PLLC
1233 20th Street, N.W.
Suite 501
Washington, DC 20036
Tel: (202) 955-3750
Fax: (202) 955-3751

In the event additional fees are necessary in connection with the filing of this paper, or if a petition for extension of time is required for timely acceptance of same, the Commissioner is hereby authorized to charge Deposit Account No. 180013 for any such fees; and applicants hereby petition for any needed extension of time.